LISTING OF THE CLAIMS

Claims 1-19 (Cancelled.)

20. (Original) A MOS transistor comprising:

a plurality of first strips of a first conductivity type, a first strip having a width that varies with length from a first width to a second larger width to the first width;

a plurality of second strips of the first conductivity type, a second strip having a width that varies with length from a third width to a fourth smaller width to the third width, a line normal to the lengths of the first strip and the second strip passes through the first width and the third width, the third width being larger than the first width;

a plurality of channel region strips, a channel region strip located between adjacent first and second strips, the channel region strip having a shape that varies with length, the shape being defined by the adjacent first and second strips; and

a plurality of gate strips, a gate strip formed over each channel region strip, the gate strip having a shape that varies with length and substantially matches the shape of the channel region strip.

21. (Previously Presented) A MOS transistor formed in a semiconductor material of a first conductivity type, the MOS transistor comprising:

a plurality of source strips of a second conductivity type formed in the semiconductor material;

a plurality of drain strips of the second conductivity type formed in the semiconductor material such that a drain strip lies between adjacent pairs of source strips;

a plurality of channel strips located between the source and drain strips such that a channel strip is located between each adjacent source and drain strip;

JKF 11/7/05

plurality of gate isolation layer

a ~~layer of isolation material~~ formed on the semiconductor material over the channel strips; and

plurality of gate isolation layer

a plurality of gate strips formed on the ~~isolation material~~ over the channel strips between source strips and drain strips.

22. (Previously Presented) The MOS transistor of claim 21 wherein a source strip has:

a center chord that lies along a longitudinal centerline of the source strip;

a first edge having a plurality of spaced-apart first points and a plurality of spaced-apart second points; and

an opposing second edge having a plurality of spaced-apart third points and a plurality of spaced-apart fourth points, each first point having a corresponding third point and being separated from the corresponding third point by a first distance measured along a first line normal to the center chord, each second point having a corresponding fourth point and being separated from the corresponding fourth point by a second distance measured along a second line normal to the center chord, the second distance being less than the first distance.

23. (Previously Presented) The MOS transistor of claim 22 wherein a second point lies between an adjacent pair of first points on the first edge.

24. (Previously Presented) The MOS transistor of claim 23 wherein a fourth point lies between an adjacent pair of third points on the second edge.

25. (Previously Presented) The MOS transistor of claim 22 and further comprising:

a layer of isolation material that contacts the semiconductor material and the source strip;

a single source metal region formed on the layer of insulation material to make electrical connections with the plurality of vias, the single source metal region covering more than 25% and less than 50% of the plurality of source and drain strips.

29. (Previously Presented) The MOS transistor of claim 22 wherein a drain strip includes:

a middle chord that lies along a longitudinal centerline of the drain strip;

a first edge having a plurality of spaced-apart fifth points and a plurality of spaced-apart sixth points; and

an opposing second edge having a plurality of spaced-apart seventh points and a plurality of spaced-apart eighth points, each fifth point having a corresponding seventh point and being separated from the corresponding seventh point by second distance measured along the first line, each sixth point having a corresponding eighth point and being separated from the corresponding eighth point by the first distance measured along the second line.

30. (Previously Presented) The MOS transistor of claim 29 wherein a sixth point lies between an adjacent pair of fifth points.

31. (Previously Presented) The MOS transistor of claim 30 wherein an eighth point lies between an adjacent pair of seventh points.

32. (Previously Presented) The MOS transistor of claim 29 and further comprising:

a layer of isolation material that contacts the semiconductor material, the source strip, and the drain strip;

a plurality of contacts formed through the layer of isolation material to make electrical connections with the source strip and the drain strip, a first number of

contacts being connected to regions of the source strip that lie between the first points and the corresponding third points, a second number of contacts being connected to regions of the drain strip that lie between the ~~fifth~~ sixth points and the corresponding ~~seventh~~ eighth points; and

a plurality of metal traces formed on the layer of isolation material to make electrical connections with the plurality of contacts.

33. (Previously Presented) The MOS transistor of claim 32 wherein no contacts are formed through the layer of isolation material to make electrical connections to regions that lie between the second and fourth points, and the fifth and seventh points.

34. (Previously Presented) The MOS transistor of claim 29 and further comprising:

a layer of isolation material that contacts the semiconductor material and the source strip;

a plurality of contacts formed through the layer of isolation material to make electrical connections with the source strip and the drain strip, the contacts being connected to each region of the source strip that lies between a first point and a corresponding third point, and each region of the drain strip that lies between a ~~fifth~~ sixth point and a corresponding ~~seventh~~ eighth point; and

a plurality of metal traces formed on the layer of isolation material to make electrical connections with the plurality of contacts.

35. (Previously Presented) The MOS transistor of claim 34 and further comprising:

a layer of insulation material that lies over the layer of isolation material and the metal traces;

specification

Thus, in accordance with the present invention, a layout has been described that utilizes a plurality of serrated gate structures that allow the source and drain regions to contacted frequently. The result is a 25% savings in space over conventional layouts.

In addition, picking up the gate strips on both ends with a layer of interconnect polysilicon and a metal-1 strip reduces the distributed RC delay associated with the gate strips (the resistance of the polysilicon strips and the capacitance under the gate strips) by a factor of two to three times.

FIGs. 7A-7B show two views that illustrate a layout 700 of PMOS transistor M0 after the metal-2 layer has been formed and patterned in accordance with the present invention. FIG. 7A shows a plan view, while FIG. 7B shows a cross-sectional view taken along lines 7B-7B of FIG. 7A. As shown in FIGs. 7A-7B, layout 700 is the same as layout 600 except that layout 700 shows the additional formation of a layer of insulation ~~isolation~~ material 710, vias 712 that are formed through isolation layer 710, and a plurality of strips of metal-2.

VCF 1/17/05

The metal-2 strips include a source strip 714, a drain strip 716, a source strip 720, and a drain strip 722. Source strip 714 is formed on insulation ~~isolation~~ material 710 to make electrical contact with the vias 712 that make an electrical connection with source strip 780.

Drain strip 716 is formed on insulation ~~isolation~~ material 710 to make electrical contact with the contacts 712 that make an electrical connection with drain strip 682. Source strip 720 is formed on insulation ~~isolation~~ material 710 to make electrical contact with the contacts 712 that make an electrical connection with p+ source strip 684.

Drain strip 722 is formed on isolation material 712 to make electrical contact with the contacts 712 that make an electrical connection with drain strip 686. (Although not shown, a metal-2